WHAT IS CLAIMED IS:

1. A signal processing circuit, comprising:

a sample/hold circuit for sampling an input signal separately inputted for a time interval of the first half and for a time interval of the second half for the time interval of the first half and for holding the inputted signal for the time interval of the second half;

a subtracter for taking a difference between the sampled and held signal and the inputted signal; and

a voltage clamp circuit for receiving as its input a signal from the subtracter,

wherein the voltage clamp circuit carries out clamping for a part of or all of the time interval of the first half.

2. A signal processing circuit according to claim 1, which receives as its input an optical signal obtained due to storage of electric charges generated due to light incident upon photoelectric converter, and a reference signal becoming a reference for the photoelectric converter, wherein

the optical signal is inputted for the time interval of the first half and the reference signal is inputted for the time interval of the second half, or the reference signal is inputted for the time interval of the first half and the optical signal is inputted for the time interval of the second half.

3. A signal processing circuit according to claim 1, further comprising a circuit for sampling a signal from the voltage clamp circuit for the time interval of the second half to hold the sampled signal.

4. A signal processing circuit according to claim 1, further comprising a gain amplifier for amplifying a signal from the voltage clamp circuit, wherein a reference voltage for the gain amplifier and a first reference voltage used to carry out the clamping in the voltage clamp circuit are common to each other.

5. A signal processing circuit according to claim 1, wherein a reference voltage for the subtracter and a first reference voltage used to carry out the clamping in the voltage clamp circuit are common to each other.

6. An image sensor IC, comprising the signal processing circuit as claimed in claim 2 which is formed together with photoelectric converter on one semiconductor substrate.

7. An image sensor, comprising the signal processing circuit and the photoelectric converter as claimed in claim 2.

8. An image sensor, comprising:

read means for reading out an optical signal and a reference signal to a common signal line, wherein the optical signal is obtained due to storage of electric charges generated due to light incident upon photoelectric converter and the reference signal is becoming a reference for the photoelectric converter;

a sample/hold circuit for receiving as its input a signal from the common signal line; and

a subtracter for taking and amplifying a difference between the sampled and held signal and the inputted signal.

9. An image sensor, comprising:

a first hold circuit for holding an optical signal obtained due to storage of electric charges generated due to light incident upon photoelectric converter;

a second hold circuit for holding a reference signal becoming a reference for the photoelectric converter;

read means for reading out the optical signal and the reference signal which are held in order to a common signal line;

a sample/hold circuit for receiving as its input a signal from the common signal line; and

a subtracter for taking and amplifying a difference between the sampled and held signal and the inputted signal.

10. An image sensor IC, comprising:

a photoelectric converter;

a signal processing circuit for receiving as its input a signal of the photoelectric converter;

a signal output terminal connected to an output terminal of the signal processing circuit;

a reference voltage terminal connected to a terminal at which a reference voltage for the signal processing circuit appears;

a reference voltage circuit; and

a resistor provided between the reference voltage circuit and the reference voltage terminal,

the signal processing circuit comprising:

a sample/hold circuit for separately receiving as its input an optical signal and a reference signal for a time interval of the first half and for a time interval of the second half to sample the inputted signal for the time interval of the first half and to hold the sampled signal for the time interval of the second half, wherein the optical signal is obtained due to storage of electric charges generated due to light incident upon a photoelectric conversion area of photoelectric converter and the reference signal is becoming a reference for the photoelectric converter;

a subtracter for taking a difference between the sampled and held signal and the inputted signal; and

a voltage clamp circuit for clamping a signal from the

subtracter for the time interval of the first half,

wherein one of a reference voltage for the voltage clamp circuit and a reference voltage for the subtracter is supplied through the reference voltage terminal.

11. A close contact type image sensor, comprising a plurality of image sensor ICs each as claimed in claim 10, wherein reference voltage terminals of the plurality of image sensor ICs are electrically connected to one another.

12. An image sensor IC according to claim 10, further comprising a gain amplifier for amplifying the clamped signal, wherein a reference voltage for the gain amplifier is supplied through the reference voltage terminal.

13. An image sensor IC, comprising:

a plurality of photoelectric converter; and

a plurality of reset switches connected to the plurality of photoelectric converter for initializing the plurality of photoelectric converter, respectively,

wherein the plurality of reset switches are electrically connected to a reference voltage terminal.

14. An image sensor IC according to claim 13, further comprising

a signal processing circuit built therein for receiving as its input output signals of the plurality of photoelectric converter, wherein a reference voltage for the signal processing circuit is supplied through the reference voltage terminal.

15. An image sensor IC according to claim 13, further comprising:

a reference voltage circuit built therein; and

a resistor provided between the reference voltage circuit and the reference voltage terminal.

16. An image sensor comprising a plurality of image sensor ICs each as claimed in claim 13, wherein the reference voltage terminals of the plurality of image sensor ICs are electrically connected to one another.

17. An image sensor IC, comprising:

a plurality of photoelectric converter;

a plurality of reset switches connected to the plurality of photoelectric converter for initializing the plurality of photoelectric converter, respectively;

a first hold circuit for holding an optical signal obtained due to storage of electric charges generated due to light incident upon the photoelectric converter;

a second hold circuit for holding a reference signal becoming a reference for the photoelectric converter; and

read means for reading out the optical signal and the reference signal which are held in order to a common signal line,

wherein the plurality of reset switches are electrically connected to a reference voltage terminal.

18. An image sensor comprising a plurality of image sensor ICs each as claimed in claim 16, wherein the reference voltage terminals of the plurality of image sensor ICs are electrically connected to one another.

19. A signal processing method for use in a signal processing circuit comprising at least: a sample/hold circuit for receiving its input an input signal having a time interval of the first half and a time interval of the second half; a subtracter for receiving as its input a signal from the sample/hold circuit and the input signal; and a voltage clamp circuit for receiving as its input a signal from the subtracter and a reference voltage, wherein:

the sample/hold circuit, for the time interval of the first half of the input signal, holds the input signal and outputs the held input signal to the subtracter;

the subtracter, for the time interval of the second half of the input signal, outputs a difference signal exhibiting a difference

between a signal from the sample/hold circuit and the input signal to the clamp circuit; and

the voltage clamp circuit, for the time interval of the first half, clamps an output signal of the voltage clamp circuit to the reference voltage, and for the time interval of the second half, superimposes the difference signal on the reference voltage.

20. A signal processing method according to claim 19, wherein an output signal from the sample/hold circuit and the input signal are amplified to be inputted to the subtracter.